We claim:

1. A method for processing a signal received from a dispersive channel, said channel having a memory length, L, and being modeled as a filter having L taps, said method comprising the steps of:

processing less significant taps with a lower complexity cancellation algorithm that cancels the less significant taps using tentative decisions; and

processing more significant taps with a reduced state sequence estimation (RSSE) technique.

Sub A2

2. The method according to claim 1, wherein said lower complexity cancellation algorithm is a decision-feedback equalizer (DFE) technique.

3. The method according to claim 1, wherein said lower complexity cancellation algorithm is a soft decision-feedback equalizer (DFE) technique.

4. The method according to claim 1, wherein said lower complexity cancellation algorithm reduces the intersymbol interference associated with said less significant taps.

5. The method according to claim 1, wherein said more significant taps comprise taps below a tap number, U, where U is a prescribed number less than L.

6. The method according to claim 1, further comprising the step of sampling said signal.

7. The method according to claim 1, further comprising the step of digitizing said signal.

11

8. The method according to claim 1, wherein said reduced state sequence estimation (RSSE) technique is a decision-feedback sequence estimation (DFSE) technique.

9. The method according to claim 1, wherein said reduced state sequence estimation (RSSE) technique is a parallel decision-feedback equalization (PDFE) technique.

Sub B3

10. A receiver that receives a signal from a dispersive channel, said channel having a memory length, L, and being modeled as a filter having L taps, comprising:

a tentative decision/tail processing circuit for processing less significant taps with a lower complexity cancellation algorithm; and

a reduced state sequence estimation (RSSE) circuit for processing only the more significant taps.

11. The receiver according to claim 10, wherein said tentative decision/tail processing circuit implements a decision-feedback equalizer (DFE) technique to cancel said less significant taps using tentative decisions.

12. The receiver according to claim 10, wherein said lower complexity cancellation algorithm is a soft decision-feedback equalizer (DFE) technique.

14 ~~13~~. The receiver according to claim 11 ~~10~~, wherein said lower complexity cancellation algorithm reduces the intersymbol interference associated with said less significant taps.

15 ~~14~~. The receiver according to claim 11 ~~10~~, wherein said more significant taps comprise taps below a predefined tap number, U, where U is less than L.

15. The receiver according to claim 10, wherein said reduced state sequence estimation (RSSE) circuit employs a decision-feedback sequence estimation (DFSE) technique.

16. The receiver according to claim 10, wherein said reduced state sequence estimation (RSSE) circuit employs a parallel decision-feedback equalization (PDFE) technique.

17. A method for processing a signal received from a dispersive channel, said channel having a memory length, L, and being modeled as a filter having L taps, said method comprising the steps of:

Sub A4

processing less significant taps with a lower complexity cancellation algorithm that cancels the less significant taps using tentative decisions; and

processing more significant taps with an M-algorithm (MA) technique.

18. A receiver that receives a signal from a dispersive channel, said channel having a memory length, L, and being modeled as a filter having L taps, comprising:

a tentative decision/tail processing circuit for processing less significant taps with a lower complexity cancellation algorithm; and

a sequence estimation circuit that implements an M-algorithm (MA) for processing only the more significant taps.

19. A method for processing a signal received from a dispersive channel, said channel having a memory length, L, and being modeled as a filter having L taps, said method comprising the steps of:

processing less significant taps with a first algorithm of first complexity; and

processing more significant taps with a second algorithm of second complexity that is greater than said first complexity.

20. A receiver that receives a signal from a dispersive channel, said channel having a memory length, L, and being modeled as a filter having L taps, comprising:

a processing circuit that processes less significant taps with a first algorithm of first complexity; and

a processing circuit that processes more significant taps with a second algorithm of second complexity that is greater than said first complexity.

Sub A1 cont'd.

21. A receiver that receives a signal from a dispersive channel, said channel having a memory length, L, and being modeled as a filter having L taps, comprising:

means for processing less significant taps with a first algorithm of first complexity; and

means for processing more significant taps with a second algorithm of second complexity that is greater than said first complexity.

22. A receiver that receives a signal from a dispersive channel, said channel having a memory length, L, and being modeled as a filter having L taps, comprising:

means for processing less significant taps with a lower complexity cancellation algorithm that cancels the less significant taps using tentative decisions; and

means for processing more significant taps with a reduced state sequence estimation (RSSE) technique.

add C1